CLAIMS

1. A CMOS imager, comprising:

   a photoconversion device; and

   a first transistor associated with said photoconversion device at a first side of said first transistor, said first transistor having a single active area extension region on a second side of said transistor opposite said first side.

2. The CMOS imager of claim 1, wherein said first transistor is a reset transistor in electrical communication with said photoconversion device.

3. The CMOS imager of claim 1, wherein said first transistor is a transfer transistor in electrical communication with said photoconversion device.

4. The CMOS imager of claim 1, wherein said first transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

5. The CMOS imager of claim 1, wherein said first transistor has a gate length which is increased relative to other transistors in electrical communication with said photoconversion device.

6. The CMOS imager of claim 1, comprising a halo implant region below said single active area extension region, said halo implant region extending partially below a gate of said first transistor.

7. The CMOS imager of claim 1, wherein said photoconversion device is one of a photodiode, a photogate, or a photoconductor.

8. The CMOS imager of claim 6, wherein said single active area extension region and said halo implant region are spaced away from a gate of said first transistor by a portion of a substrate supporting said first transistor.

9. The CMOS imager of claim 1, wherein said photoconversion device is part of a four transistor pixel circuit comprising a transfer transistor as said first transistor, a reset transistor, a source follower transistor, and a row select transistor.

10. The CMOS imager of claim 9, wherein at least one of said reset transistor and said source follower transistor have a single active area extension region.

11. The CMOS imager of claim 1, wherein said photoconversion device is part of a three transistor circuit comprising a reset transistor as said first transistor, a source follower transistor, and a row select transistor.

12. The CMOS imager of claim 11, wherein said source follower transistor has a single active area extension region.

13. The CMOS imager of claim 1, wherein said active area extension region of said first transistor has a dopant concentration of about 1 x 10^{12} to about 3 x 10^{13} ions/cm^2.

14. The CMOS imager of claim 1, wherein said first transistor has a single insulating spacer, said spacer positioned on said second side of said transistor.

15. A pixel sensor cell, comprising:

a semiconductor substrate;

a transfer transistor over said substrate, said transfer transistor having a single active area extension region located on a first side of said transfer transistor;

a photosensor in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side;

a reset transistor gate over said substrate and spaced apart from said transfer transistor; and

a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region in electrical communication with said active area extension region.

16. The pixel sensor cell of claim 15, wherein said transfer transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

17. The pixel sensor cell of claim 15, wherein said transfer transistor has a gate length which is increased relative to other transistor gates in electrical communication with said photosensor.

18. The pixel sensor cell of claim 15, wherein said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor gate.

19. The pixel sensor cell of claim 15, wherein said reset transistor comprises a single active area extension region on a side opposite said floating diffusion region.

20. The pixel sensor cell of claim 15, further comprising at least a source follower transistor and a row select transistor.

21. A pixel sensor cell, comprising:

a semiconductor substrate;

a reset transistor over said substrate;

a photosensor in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor;

a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side; and

a halo implant region in said substrate below said single active area extension region.

22. The pixel sensor cell of claim 21, wherein said reset transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

23. The pixel sensor cell of claim 21, wherein said reset transistor has a gate length which is increased relative to other transistor gates in electrical communication with said photosensor.

24. The pixel sensor cell of claim 21, wherein said photosensor and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor and a row select transistor.

25. The pixel sensor cell of claim 22, wherein said single active area extension region of said reset transistor is a lightly doped drain.

26. An image sensor, comprising:

a semiconductor substrate;

a reset transistor over said substrate;

a floating diffusion region in said substrate and in electrical communication with said reset transistor at a first of said reset transistor;

a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a second side of said reset transistor which is opposite to said first side; and

a halo implant region in said substrate below said single active area extension region.

27. The image sensor of claim 26, wherein the image sensor is a CMOS imager.

28. The image sensor of claim 27, further comprising a photodiode in electrical contact with said reset transistor, said photodiode being within said substrate on said first side of said reset transistor.

29. The image sensor of claim 27, wherein said floating diffusion region is located within a sensor array.

30. The image sensor of claim 26, wherein the image sensor is a CCD imager.

31. The image sensor of claim 29, wherein said floating diffusion region is located outside a sensory array.

32. An imager device, comprising:

an image processor; and

a pixel array for supplying signals to said image processor, at least one pixel of said array comprising:

a photoconversion device, and

a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said transistor gate having a single lightly doped drain on a second side of said transistor gate opposite said first side.

33. The imager device of claim 32, wherein said first transistor gate is of a reset transistor in electrical communication with said photoconversion device.

34. The imager device of claim 32, wherein said first transistor gate is of a transfer transistor in electrical communication with said photoconversion device.

35. The imager device of claim 32, wherein said first transistor gate has an underlying channel region, said channel region having a threshold voltage adjustment implant.

36. The imager device of claim 32, wherein said first transistor gate has a length which is increased relative to other transistor gates in electrical communication with said photoconversion device.

37. The imager device of claim 32, wherein said photoconversion device is a photodiode.

38. A semiconductor transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a side of said transistor opposite from said photodiode.

39. The semiconductor transistor of claim 38, further comprising a threshold voltage adjustment implant below a gate of said transistor.

40. The semiconductor transistor of claim 38, wherein said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same pixel.

41. The semiconductor transistor of claim 38, further comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

42. The semiconductor transistor of claim 38, further comprising an insulating layer over said transistor and said photodiode, said insulating layer extending to a floating diffusion region adjacent to said active area extension region.

43. The semiconductor transistor of claim 38, wherein said transistor and said photodiode are part of a CMOS imager pixel.

44. The semiconductor transistor of claim 38, wherein said transistor and said photodiode are part of a CCD imager.

45. The semiconductor transistor of claim 38, wherein said transistor is part of a pixel having at least two other transistors in electrical communication with said photodiode.

46. A semiconductor transistor in electrical contact with a photodiode, said transistor having a gate length which is increased relative to any other transistor gate length of transistors of a same pixel.

47. The semiconductor transistor of claim 46, wherein said transistor comprises a single active area extension region on a opposite side of said transistor from said photodiode.

48. The semiconductor transistor of claim 47, comprising a threshold voltage adjustment implant below a gate of said transistor.

49. The semiconductor transistor of claim 47, comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor by a portion of a substrate supporting said transistor by a portion of a substrate supporting said transistor.

50. A semiconductor transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a opposite side of said transistor from said photodiode and a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor.

51. The semiconductor transistor of claim 50, further comprising a threshold voltage adjustment implant below a gate of said transistor.

52. The semiconductor transistor of claim 51, wherein said transistor has a gate length which is increased relative to any other transistor gate length of transistors of a same pixel.

53. A method of forming a pixel of an imager device, comprising:

forming a photoconversion device in a substrate;

forming a first transistor gate stack over said substrate adjacent said photoconversion device at a first side of said first transistor gate; and

forming a single active area extension region in said substrate adjacent to said first transistor gate stack on a second side thereof, which is opposite from said first side.

54. The method of claim 53, wherein said photoconversion device is a photodiode.

55. The method of claim 54, wherein said forming said single active area extension region comprises a self-aligned dopant implant utilizing said first transistor gate stack for alignment and a mask for preventing implantation of said dopant on said first side of said first transistor gate stack.

56. The method of claim 55, wherein said mask partially exposes said first transistor gate stack at said second side.

57. The method of claim 53, further comprising forming a floating diffusion region within said substrate, said floating diffusion region being separated from said first transistor gate stack by said active area extension region.

58. The method of claim 57, wherein said floating diffusion region and said active area extension region are spaced away from said first transistor gate stack by a portion of said substrate.

59. The method of claim 53, further comprising performing a threshold voltage adjustment implant in said substrate under said first transistor gate stack.

60. The method of claim 53, wherein said first transistor gate stack has a gate length that is increased relative to other transistors of the same said pixel.

61. The method of claim 53, wherein said forming a single active area extension region comprises implanting a dopant at a concentration of about 1×10^{12} to about 3×10^{13} ions/cm^2.

62. The method of claim 53, further comprising forming a halo implant region below said active area extension region.

63. The method of claim 53, further comprising forming a reset transistor, a source follower transistor, and a row select transistor in the same circuit as said photodiode and said first transistor gate.

64. The method of claim 63, further comprising forming a single active area extension region at each of said reset transistor and said source follower transistor.

65. A method of forming an array of pixels isolated from one another within and on a substrate, comprising:

forming a photodiode within said substrate;

forming a transfer transistor gate over said substrate and in electrical communication with said photodiode;

forming a reset transistor gate over said substrate and spaced apart from said transfer transistor gate;

implanting a first dopant to form active area extension regions in said substrate on both sides of said reset transistor gate and on one side of said transfer transistor gate opposite from said photodiode;

implanting a second dopant to form halo implant regions below said active area extension regions;

forming an insulating layer over said transfer transistor gate and said reset transistor gate at least over said active area extension regions; and

implanting a third dopant in said substrate to form a floating diffusion region between said transfer transistor gate and said reset transistor gate and a source/drain region adjacent to a side of reset transistor gate opposite said floating diffusion region.

66. The method of claim 65, wherein said insulating layer covers said transfer transistor gate, said photodiode, and sides of said reset transistor gate.

67. The method of claim 66, wherein said active area extension region on one side of said transfer transistor gate and said floating diffusion region are spaced away from said transfer transistor gate by a portion of said substrate.

68. The method of claim 65, further comprising performing a threshold voltage adjustment implant for said transfer transistor gate.

69. The method of claim 65, wherein said transfer transistor gate is formed having a gate length which is increased relative to other transistors of said pixel.

70. A method of forming an array of pixels isolated from one another within and over a substrate, comprising:

forming a photodiode within said substrate;

forming a reset transistor gate over said substrate and in electrical communication with said photodiode;

implanting a first dopant to form an active area extension region in said substrate on one side of said reset transistor gate which is opposite from said photo diode;

implanting a second dopant to form a halo implant region in said substrate below said active area extension region;

forming an insulating layer over at least a portion of said reset transistor gate; and

implanting a third dopant in said substrate to form a source and drain region adjacent to a side of reset transistor gate opposite said photodiode.

71. The method of claim 70, further comprising performing a threshold voltage adjustment implant for said reset transistor gate.

72. The method of claim 70, wherein said reset transistor gate is formed having a gate length which is increased relative to other transistors of said pixel.

73. A method of forming an imager pixel with mitigated dark current leakage, comprising forming a transistor adjacent a photodiode at a first side of said transistor, said transistor having a single active area extension region at a second side of said transistor opposite said first side.

74. The method of claim 73, further comprising forming an active area adjacent said single active area extension region.

75. The method of claim 74, wherein said active area and said active area extension region are spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

76. The method of claim 73, wherein said transistor has an increased gate length relative to any other transistor gate said imager pixel.

77. The method of claim 73, further comprising providing a threshold voltage adjustment implant below said transistor.

78. A method of forming an imager pixel with mitigated leakage and dark current, comprising forming a transistor adjacent a photodiode at a first side of said transistor, said transistor having a single active area extension region at a second side of said transistor opposite said first side and a threshold voltage adjustment implant below said transistor.

79. The method of claim 78, wherein said transistor has an increased gate length relative to any other transistor gate said imager pixel.

80. A method of forming an imager pixel with mitigated leakage and dark current, comprising forming a transistor adjacent a photodiode at a first side of said transistor, said transistor having a single active area extension region at a second side of said transistor opposite said first side and where said transistor has an increased gate length relative to any other transistor gate said imager pixel.

81. The method of claim 80, further comprising providing a threshold voltage adjustment implant below said transistor.

82. A method of forming an imager pixel with mitigated leakage and dark current, comprising forming a transistor adjacent a photodiode at a first side of said transistor, said transistor having an active area and a single active area extension region at a second side of said transistor opposite said first side, where said active area and said active area extension region are spaced away from a gate of said transistor by a portion of a substrate supporting said transistor

83. The method of claim 82, where said transistor has an increased gate length relative to any other transistor gate said imager pixel.

84. The method of claim 82, further comprising providing a threshold voltage adjustment implant below said transistor..

85. A semiconductor transistor comprising a channel region between a higher voltage side and a lower voltage side, and a single active area extension region at said higher voltage side of said channel, said transistor being associated with circuitry of a photoimaging circuit.

86. The semiconductor transistor of claim 85, wherein said transistor is part of a pixel.

87. The semiconductor transistor of claim 85, wherein said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same photoimager circuit.

88. The semiconductor transistor of claim 85, further comprising a threshold voltage adjustment implant below a gate of said transistor.

89. The semiconductor transistor of claim 85, wherein said transistor is associated with a photodiode of a CMOS imager pixel.

90. The semiconductor transistor of claim 85, wherein said transistor is part of a CCD imager.

91. A CCD imager comprising at least one transistor gate with a single active area extension region at a higher voltage side of said at least one transistor gate.

92. The CCD imager of claim 91, wherein said at least one transistor gate is of a reset transistor.

93. The CCD imager of claim 91, wherein said at least one transistor gate is of a source follower transistor.